What Is Claimed Is:

1. A method of sharing a line bandwidth on a communication path among a plurality of virtual circuits in an ATM Device, said line bandwidth equaling a line rate, wherein said plurality of virtual circuits comprise a plurality of VC-types, said method comprising:

accepting a configuration of said plurality of virtual circuits, wherein a sum of allocated bandwidths of said plurality of virtual circuits exceeds said line rate;

receiving a plurality of cells on said plurality of virtual circuits; and

scheduling for transmission said plurality of cells on said communication path while enforcing a pre-specified priority with respect to said plurality of VC-types and while limiting bandwidth usage by each of said plurality of virtual circuits to a corresponding allocated bandwidth.

2. The method of claim 1, wherein said plurality of VC-types comprise constant bit rate (CBR) VC-type, variable bit rate-real time (VBR-RT) VC-type, variable bit rate - non real time (VBR-nRT) VC-type, wherein said pre-specified priority comprises highest to lowest priority for CBR VC-type, VBR-RT VC-type and VBR-nRT VC-type in that order, wherein a first cell related to a lower priority VC-type is scheduled for transmission only if no cells of a higher priority VC-type are ready for transmission.

3. The method of claim 2, wherein said plurality of VC-types further comprises unspecified bit rate (UBR) VC-type, wherein UBR VC-type is given lower priority than

said VBR-nRT VC-type.

4. The method of claim 2, wherein said scheduling comprises:

determining cell slots in which of each of said plurality of virtual circuits is a candidate for allocation according to a corresponding allocated bandwidth, wherein a first virtual circuit of a first VC-type and a second virtual circuit of a second VC-type are determined to be candidates for allocation in a first cell slot on said communication path, wherein said first VC-type is different from said second VC-type; and

allocating said first cell slot to one of said first virtual circuit and said second virtual circuit having a higher priority if the virtual circuit with the higher priority has a cell ready for transmission.

5. The method of claim 4, wherein said scheduling further comprises allocating said first cell slot to one of said first virtual circuit and said second virtual circuit having a lower priority if the virtual circuit with the higher priority does not have a cell ready for transmission and if the virtual circuit with the lower priority has a cell ready for transmission.

6. The method of claim 5, wherein said scheduling further comprises:

maintaining a VC-credit counter associated with a fourth virtual circuit comprised in said plurality of virtual circuits, wherein said VC-credit counter indicates a number of cells of backlog for said fourth virtual circuit according to the corresponding allocated

bandwidth, but limited by a maximum number specified by a VC-type of said fourth virtual circuit, wherein each cell slot on said communication path is allocated to said fourth virtual circuit only if said VC-credit counter is at least greater than or equal to one.

7. The method of claim 6, wherein said maintaining comprises:

initializing said VC-credit counter and a line slot credit counter associated with said fourth virtual circuit to zero;

computing an inter-cell delay associated with said fourth virtual circuit according to the corresponding allocated bandwidth; and

incrementing said line slot credit counter by a token value in each cell slot of said communication path, wherein said token value is determined by a length of duration of cell slots on said communication path;

incrementing said VC-credit counter by one if said line slot credit counter is equal to or greater than said inter-cell delay and if said VC-credit counter is already not equal to said maximum number;

decrementing said line slot credit counter by said inter-cell delay when said VC-credit counter is incremented; and

decrementing said VC-credit counter by one when a cell related to said fourth virtual circuit is scheduled for transmission.

8. The method of claim 7, further comprising:

computing a peak maximum slot credit and a peak intercell delay associated with

a fifth virtual circuit, wherein said peak intercell delay and said peak maximum slot credit are computed according to a corresponding peak cell rate (PCR);

initializing a peak slot credit associated with said fifth virtual circuit to zero;

incrementing said peak slot credit by said token value in each cell slot, but said peak slot credit being capped at said peak maximum slot credit;

decrementing said peak slot credit by said peak intercell delay if a cell associated with said fifth virtual circuit is scheduled for transmission; and

scheduling for transmission a cell on said fifth virtual circuit only if said peak slot credit is greater than or equal to said peak intercell delay.

9. The method of claim 8, wherein said fourth virtual circuit is of CBR VC-type, and wherein said maximum number equals 1.

10. The method of claim 8, wherein said fourth virtual circuit is the same as said fifth virtual circuit and is of VBR VC-type, and wherein said maximum number is computed according to the equation [MBS - (MBS x SCR/PCR) - 1], wherein - and x respectively represent a subtraction and a multiplication operation, PCR represents peak cell rate, SCR represents sustained cell rate, and MBS represents maximum burst size of said fourth virtual circuit.

11. The method of claim 8, wherein said ATM device comprises one of a CPE, an ATM switch and a edge router.

12. A machine readable medium carrying one or more sequences of instructions for causing an ATM device to share a line bandwidth on a communication path among a plurality of virtual circuits, said line bandwidth equaling a line rate, wherein said plurality of virtual circuits comprise a plurality of VC-types, wherein execution of said one or more sequences of instructions by one or more processors contained in said ATM device causes said one or more processors to perform the actions of:

accepting a configuration of said plurality of virtual circuits, wherein a sum of allocated bandwidths of said plurality of virtual circuits exceeds said line rate;

receiving a plurality of cells on said plurality of virtual circuits; and

scheduling for transmission said plurality of cells on said communication path while enforcing a pre-specified priority with respect to said plurality of VC-types and while limiting bandwidth usage by each of said plurality of virtual circuits to a corresponding allocated bandwidth.

13. The machine readable medium of claim 12, wherein said plurality of VC-types comprise constant bit rate (CBR) VC-type, variable bit rate-real time (VBR-RT) VC-type, variable bit rate - non real time (VBR-nRT) VC-type, wherein said pre-specified priority comprises highest to lowest priority for CBR VC-type, VBR-RT VC-type and VBR-nRT VC-type in that order, wherein a first cell related to a lower priority VC-type is scheduled for transmission only if no cells of a higher priority VC-type are ready for transmission.

14. The machine readable medium of claim 13, wherein said plurality of VC-types further comprises unspecified bit rate (UBR) VC-type, wherein UBR VC-type is given lower priority than said VBR-nRT VC-type.

15. The machine readable medium of claim 13, wherein said scheduling comprises:

determining cell slots in which of each of said plurality of virtual circuits is a candidate for allocation according to a corresponding allocated bandwidth, wherein a first virtual circuit of a first VC-type and a second virtual circuit of a second VC-type are determined to be candidates for allocation in a first cell slot on said communication path, wherein said first VC-type is different from said second VC-type; and

allocating said first cell slot to one of said first virtual circuit and said second virtual circuit having a higher priority if the virtual circuit with the higher priority has a cell ready for transmission.

16. The machine readable medium of claim 15, wherein said scheduling further comprises allocating said first cell slot to one of said first virtual circuit and said second virtual circuit having a lower priority if the virtual circuit with the higher priority does not have a cell ready for transmission and if the virtual circuit with the lower priority has a cell ready for transmission.

17. The machine readable medium of claim 16, wherein said scheduling further

comprises:

maintaining a VC-credit counter associated with a fourth virtual circuit comprised in said plurality of virtual circuits, wherein said VC-credit counter indicates a number of cells of backlog for said fourth virtual circuit according to the corresponding allocated bandwidth, but limited by a maximum number specified by a VC-type of said fourth virtual circuit, wherein each cell slot on said communication path is allocated to said fourth virtual circuit only if said VC-credit counter is at least greater than or equal to one.

18. The machine readable medium of claim 17, wherein said maintaining comprises:

initializing said VC-credit counter and a line slot credit counter associated with said fourth virtual circuit to zero;

computing an inter-cell delay associated with said fourth virtual circuit according to the corresponding allocated bandwidth; and

incrementing said line slot credit counter by a token value in each cell slot of said communication path, wherein said token value is determined by a length of duration of cell slots on said communication path;

incrementing said VC-credit counter by one if said line slot credit counter is equal to or greater than said inter-cell delay and if said VC-credit counter is already not equal to said maximum number;

decrementing said line slot credit counter by said inter-cell delay when said VC-credit counter is incremented; and

decrementing said VC-credit counter by one when a cell related to said fourth virtual circuit is scheduled for transmission.

19. The machine readable medium of claim 18, further comprising:

computing a peak maximum slot credit and a peak intercell delay associated with a fifth virtual circuit, wherein said peak intercell delay and said peak maximum slot credit are computed according to a corresponding peak cell rate (PCR);

initializing a peak slot credit associated with said fifth virtual circuit to zero;

incrementing said peak slot credit by said token value in each cell slot, but said peak slot credit being capped at said peak maximum slot credit;

decrementing said peak slot credit by said peak intercell delay if a cell associated with said fifth virtual circuit is scheduled for transmission; and

scheduling for transmission a cell on said fifth virtual circuit only if said peak slot credit is greater than or equal to said peak intercell delay.

20. The machine readable medium of claim 19, wherein said fourth virtual circuit is of CBR VC-type, and wherein said maximum number equals 1.

21. The machine readable medium of claim 19, wherein said fourth virtual circuit is the same as said fifth virtual circuit and is of VBR VC-type, and wherein said maximum number is computed according to the equation [MBS - (MBS x SCR/PCR) - 1], wherein - and x respectively represent a subtraction and a multiplication operation,

PCR represents peak cell rate, SCR represents sustained cell rate, and MBS represents maximum burst size of said fourth virtual circuit.

22. The machine readable medium of claim 19, wherein said ATM device comprises one of a CPE, an ATM switch and a edge router.

23. An ATM device sharing a line bandwidth on a communication path among a plurality of virtual circuits, said line bandwidth equaling a line rate, wherein said plurality of virtual circuits comprise a plurality of VC-types, said ATM device comprising:

means for accepting a configuration of said plurality of virtual circuits, wherein a sum of allocated bandwidths of said plurality of virtual circuits exceeds said line rate;

means for receiving a plurality of cells on said plurality of virtual circuits; and

means for scheduling for transmission said plurality of cells on said communication path while enforcing a pre-specified priority with respect to said plurality of VC-types and while limiting bandwidth usage by each of said plurality of virtual circuits to a corresponding allocated bandwidth.

24. The ATM device of claim 23, wherein said plurality of VC-types comprise constant bit rate (CBR) VC-type, variable bit rate-real time (VBR-RT) VC-type, variable bit rate - non real time (VBR-nRT) VC-type, wherein said pre-specified priority comprises highest to lowest priority for CBR VC-type, VBR-RT VC-type and VBR-nRT VC-type in that order, wherein a first cell related to a lower priority VC-type is scheduled

for transmission only if no cells of a higher priority VC-type are ready for transmission.

25. The ATM device of claim 24, wherein said plurality of VC-types further comprises unspecified bit rate (UBR) VC-type, wherein UBR VC-type is given lower priority than said VBR-nRT VC-type.

26. The ATM device of claim 24, wherein said means for scheduling is operable to:

determine cell slots in which of each of said plurality of virtual circuits is a candidate for allocation according to a corresponding allocated bandwidth, wherein a first virtual circuit of a first VC-type and a second virtual circuit of a second VC-type are determined to be candidates for allocation in a first cell slot on said communication path, wherein said first VC-type is different from said second VC-type; and

allocate said first cell slot to one of said first virtual circuit and said second virtual circuit having a higher priority if the virtual circuit with the higher priority has a cell ready for transmission.

27. The ATM device of claim 26, wherein said means for scheduling is further operable to allocate said first cell slot to one of said first virtual circuit and said second virtual circuit having a lower priority if the virtual circuit with the higher priority does not have a cell ready for transmission and if the virtual circuit with the lower priority has a cell ready for transmission.

28. The ATM device of claim 27, wherein said means for scheduling comprises a means for maintaining a VC-credit counter associated with a fourth virtual circuit comprised in said plurality of virtual circuits, wherein said VC-credit counter indicates a number of cells of backlog for said fourth virtual circuit according to the corresponding allocated bandwidth, but limited by a maximum number specified by a VC-type of said fourth virtual circuit, wherein each cell slot on said communication path is allocated to said fourth virtual circuit only if said VC-credit counter is at least greater than or equal to one.

29. The ATM device of claim 28, wherein said means for maintaining is operable to:

initialize said VC-credit counter and a line slot credit counter associated with said fourth virtual circuit to zero;

compute an inter-cell delay associated with said fourth virtual circuit according to the corresponding allocated bandwidth; and

increment said line slot credit counter by a token value in each cell slot of said communication path, wherein said token value is determined by a length of duration of cell slots on said communication path;

increment said VC-credit counter by one if said line slot credit counter is equal to or greater than said inter-cell delay and if said VC-credit counter is already not equal to said maximum number;

decrement said line slot credit counter by said inter-cell delay when said VC-credit counter is incremented; and

decrement said VC-credit counter by one when a cell related to said fourth virtual circuit is scheduled for transmission.

30. The ATM device of claim 29, wherein said means for maintaining is operable to:

computing a peak maximum slot credit and a peak intercell delay associated with a fifth virtual circuit, wherein said peak intercell delay and said peak maximum slot credit are computed according to a corresponding peak cell rate (PCR);

initializing a peak slot credit associated with said fifth virtual circuit to zero;

incrementing said peak slot credit by said token value in each cell slot, but said peak slot credit being capped at said peak maximum slot credit;

decrementing said peak slot credit by said peak intercell delay if a cell associated with said fifth virtual circuit is scheduled for transmission; and

scheduling for transmission a cell on said fifth virtual circuit only if said peak slot credit is greater than or equal to said peak intercell delay.

31. The ATM device of claim 30, wherein said fourth virtual circuit is of CBR VC-type, and wherein said maximum number equals 1.

32. The ATM device of claim 30, wherein said fourth virtual circuit is the same

as said fifth virtual circuit and is of VBR VC-type, and wherein said maximum number is computed according to the equation [MBS - (MBS x SCR/PCR) - 1], wherein - and x respectively represent a subtraction and a multiplication operation, PCR represents peak cell rate, SCR represents sustained cell rate, and MBS represents maximum burst size of said fourth virtual circuit.

33. The ATM device of claim 30, wherein said ATM device comprises one of a CPE, a DSLAM, an ATM switch and a edge router.

34. An ATM device sharing a line bandwidth on a communication path among a plurality of virtual circuits, said line bandwidth equaling a line rate, wherein said plurality of virtual circuits comprise a plurality of VC-types, said ATM device comprising:

a memory storing data representing a configuration of said plurality of virtual circuits, wherein a sum of allocated bandwidths of said plurality of virtual circuits exceeds said line rate;

an inbound interface receiving a plurality of cells on said plurality of virtual circuits; and

a scheduler block scheduling for transmission said plurality of cells on said communication path while enforcing a pre-specified priority with respect to said plurality of VC-types and while limiting bandwidth usage by each of said plurality of virtual circuits to a corresponding allocated bandwidth.

35. The ATM device of claim 34, wherein said plurality of VC-types comprise constant bit rate (CBR) VC-type, variable bit rate-real time (VBR-RT) VC-type, variable bit rate - non real time (VBR-nRT) VC-type, wherein said pre-specified priority comprises highest to lowest priority for CBR VC-type, VBR-RT VC-type and VBR-nRT VC-type in that order, wherein a first cell related to a lower priority VC-type is scheduled for transmission only if no cells of a higher priority VC-type are ready for transmission.

36. The ATM device of claim 35, wherein said plurality of VC-types further comprises unspecified bit rate (UBR) VC-type, wherein UBR VC-type is given lower priority than said VBR-nRT VC-type.

37. The ATM device of claim 35, wherein said scheduler block is operable to:

determine cell slots in which of each of said plurality of virtual circuits is a candidate for allocation according to a corresponding allocated bandwidth, wherein a first virtual circuit of a first VC-type and a second virtual circuit of a second VC-type are determined to be candidates for allocation in a first cell slot on said communication path, wherein said first VC-type is different from said second VC-type; and

allocate said first cell slot to one of said first virtual circuit and said second virtual circuit having a higher priority if the virtual circuit with the higher priority has a cell ready for transmission.

38. The ATM device of claim 37, wherein said scheduler block is further operable

to allocate said first cell slot to one of said first virtual circuit and said second virtual circuit having a lower priority if the virtual circuit with the higher priority does not have a cell ready for transmission and if the virtual circuit with the lower priority has a cell ready for transmission.

39. The ATM device of claim 38, wherein said scheduler block is further operable to maintain a VC-credit counter associated with a fourth virtual circuit comprised in said plurality of virtual circuits, wherein said VC-credit counter indicates a number of cells of backlog for said fourth virtual circuit according to the corresponding allocated bandwidth, but limited by a maximum number specified by a VC-type of said fourth virtual circuit, wherein each cell slot on said communication path is allocated to said fourth virtual circuit only if said VC-credit counter is at least greater than or equal to one.

40. The ATM device of claim 39, wherein to maintain said VC-credit, said scheduler block is operable to:

initialize said VC-credit counter and a line slot credit counter associated with said fourth virtual circuit to zero;

compute an inter-cell delay associated with said fourth virtual circuit according to the corresponding allocated bandwidth; and

increment said line slot credit counter by a token value in each cell slot of said communication path, wherein said token value is determined by a length of duration of cell slots on said communication path;

increment said VC-credit counter by one if said line slot credit counter is equal to or greater than said inter-cell delay and if said VC-credit counter is already not equal to said maximum number;

decrement said line slot credit counter by said inter-cell delay when said VC-credit counter is incremented; and

decrement said VC-credit counter by one when a cell related to said fourth virtual circuit is scheduled for transmission.

41. The ATM device of claim 40, wherein said scheduler block is operable to:

compute a peak maximum slot credit and a peak intercell delay associated with a fifth virtual circuit, wherein said peak intercell delay and said peak maximum slot credit are computed according to a corresponding peak cell rate (PCR);

initialize a peak slot credit associated with said fifth virtual circuit to zero;

increment said peak slot credit by said token value in each cell slot, but said peak slot credit being capped at said peak maximum slot credit;

decrement said peak slot credit by said peak intercell delay if a cell associated with said fifth virtual circuit is scheduled for transmission; and

schedule for transmission a cell on said fifth virtual circuit only if said peak slot credit is greater than or equal to said peak intercell delay.

42. The ATM device of claim 41, wherein said fourth virtual circuit is of CBR VC-type, and wherein said maximum number equals 1.

43. The ATM device of claim 41, wherein said fourth virtual circuit is the same as said fifth virtual circuit and is of VBR VC-type, and wherein said maximum number is computed according to the equation [MBS - (MBS x SCR/PCR) - 1], wherein - and x respectively represent a subtraction and a multiplication operation, PCR represents peak cell rate, SCR represents sustained cell rate, and MBS represents maximum burst size of said fourth virtual circuit.

44. The ATM device of claim 41, wherein said ATM device comprises one of a CPE, a DSLAM, an ATM switch and a edge router.

45. The ATM device of claim 41, wherein said fifth virtual circuit is of UBR type.